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PATENT & TRADEMARK OFFICE

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501.37436CV2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	S. NISHIHARA et al.
Application No.:	10/721,902
Filed:	November 26, 2003
For:	METHOD OF FABRICATING SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
Art Unit:	2812
Examiner:	L. Gurley

RESPONSE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

August 16, 2004

Sir:

In response to the Office Action mailed May 14, 2004, Applicants respectfully submit the following remarks, and enclosed Terminal Disclaimer. As will be shown in the following, it is respectfully submitted that the enclosed Terminal Disclaimer overcomes the obviousness-type double patenting rejection set forth in Item 3 on page 2 of the Office Action mailed May 14, 2004, the sole rejection of claims in this Office Action mailed May 14, 2004, such that all of the presently pending claims should be allowed and the above-identified application passed to issue.

Thus, in Item 3 on page 2 of the Office Action mailed May 14, 2004, the Examiner has rejected all of the presently pending claims under the judicially created doctrine of obviousness-type double patenting, as being unpatentable over claims 1-13 of U.S. Patent No. 6,693,001. In Item 2 on page 2 of this Office Action mailed May 14, 2004, the Examiner indicates that this obviousness-type double patenting